Sheet 1 of 1

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. 501.43228X00	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT MURATA, et al.	
		FILING DATE January 14, 2004	GROUP

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
[illegible]	AA	5,198,683	03/30/1993	SIVAN	357	67	05/03/1991
[illegible]	AB	5,670,803	09/23/1997	BEILSTEIN, Jr. et al.	257	278	02/08/1995
[illegible]	AC	5,994,735	11/30/1999	MAEDA, et al.	257	329	11/30/1999
[illegible]	AD	5,627,390	05/06/1997	MAEDA, et al.	257	302	05/06/1997
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Abstract Yes	Abstract No
[illegible]	AM	11-176936	07/02/1999	JP	H01L	21/768	X	
	AN	9-232447	09/05/1997	JP	H01L	21/8244	X	
	AO	2001-28443	01/30/2001	JP	H01L	29/786	X	
	AP	6-104405	4/15/1994	JP	H01L	27/11	X	
	AQ	03/019663	03/06/2003	WO	H01L	27/11		
[illegible]	AR	00/70683	11/23/2000	WO	H01L	27/108		
	AS							
	AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

[illegible]	AU	WATANABE, et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995
	AV	
	AW	
	AX	
	AY	
	AZ	

Examiner	Date Considered
[signature]	07/05/05